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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,106	03/05/2002	John Commander	CEDE 2036	5919

321 7590 02/09/2007

SENNIGER POWERS
ONE METROPOLITAN SQUARE
16TH FLOOR
ST LOUIS, MO 63102

EXAMINER	
WONG, EDNA	
ART UNIT	**PAPER NUMBER**
1753	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	02/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 02/09/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspatents@senniger.com

Office Action Summary	Application No.	Applicant(s)	
	10/091,106	COMMANDER ET AL.	
	Examiner	Art Unit	
	Edna Wong	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,17 and 65-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,17 and 65-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

This is in response to the Amendment dated December 18, 2006. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Response to Arguments

Claim Rejections - 35 USC § 112

Claims **1-7, 17 and 65-73** have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The rejection of claims 1-7, 17 and 65-73 under 35 U.S.C. 112, second paragraph, has been withdrawn in view of Applicants' amendment.

Claim Rejections - 35 USC § 103

I. Claims **1-7 and 65-71** have been rejected under 35 U.S.C. 103(a) as being unpatentable over **Creutz, deceased et al.** (US Patent No. 4,110,176) in combination with **Barstad et al.** (US Patent No. 6,444,110 B2).

The rejection of claims 1-7 and 65-71 under 35 U.S.C. 103(a) as being unpatentable over Creutz, deceased et al. in combination with Barstad et al. is as applied in the Office Action dated June 16, 2006 and incorporated herein. The rejection has been maintained for the following reasons:

Applicants state that in view of the disparate purposes of a PCB substrate such

as contemplated by Creutz et al. and the semiconductor integrated circuit substrate of claim 1, as well as their disparate properties and functions, applicants' respectfully submit that it cannot fairly be deemed to have been obvious to "have modified the circuit device substrate described by Creutz with wherein the circuit device substrate is a semiconductor integrated circuit device substrate having electrical interconnect features ..." as asserted in the Office action.

In response, the Examiner maintains that Barstad's teaching of:

copper plating has been employed on circuit board manufacturing to plate outer layers where final circuitry is defined. More recently, copper plating has been employed in semiconductor chip manufacture to provide chip interconnections (col. 1, lines 36-65; and col. 7, lines 56-65). Conventional copper plating systems can be suitable for plating vias and trenches as small as 300 nm with 4:1 aspect ratios (col. 2, lines 20-25). Barstad shows the copper electroplating of through hole walls of a printed circuit board substrate (col. 8, Example 1) and the copper electroplating of microvias of a semiconductor microchip wafer (col. 8, Example 2) using similar copper electroplating baths

would have motivated one having ordinary skill in the art to have substituted the printed circuit board disclosed by Creutz with a semiconductor integrated circuit device substrate. The purpose or intended used of the substrates does not result in the methodological difference (or manipulative difference) between the claimed invention and the prior art.

Applicants state that that the proposed modification is also not obvious because, as emphasized in MPEP 2143.01(V), a proposed modification is not obvious if it renders the prior art unsatisfactory for its intended purpose. Semiconductor integrated circuit

substrates do not have the flexibility, workability, or density of resinous PCB substrates, and therefore are unsatisfactory for the intended purpose of PCBs.

In response, the Examiner's purposed modification does not render Creutz unsatisfactory for its intended purpose because Creutz teaches that the baths have been found particularly well adapted for *throughhole plating*, and thus, find appreciable utilization in the manufacture of printed circuit boards (col. 2, lines 20-23). The method disclosed by Barstad is not limited to the manufacturing of printed circuit boards because it can also be adapted for the manufacturing of semiconductor integrated circuits which is also a throughhole plating as taught by Barstad (col. 3, lines 49-61).

The disclosure of reference must be considered for what it fairly teaches one of ordinary skill in the art, pertinence of non-preferred disclosure must be reviewed in such light. *In re Meinhardt* 157 USPQ 270; and MPEP § 2123 and § 2141.02(VI).

Applicants state that for a proposed combination to be obvious, there must be some reasonable expectation of success, per MPEP 2143.02. The various properties of semiconductor integrated circuit substrates -- e.g., silicon wafers -- are so distinct from the properties of PCB substrates -- e.g., epoxy-based resins -- that there is no reasonable technical basis to conclude the proposed modification would be successful.

In response, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the

references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Furthermore, there is no reason why the copper electroplating baths disclosed by Creutz would not deposit copper on a semiconductor integrated circuit substrate when Barstad successfully electroplated copper on the through hole walls of a printed circuit boar substrate (col. 8, Example 1) and in the microvias of a semiconductor chip wafer (col. 2, Example 2) with copper electroplating baths comprising $CuSO_4 \cdot H_2O$, H_2SO_4, Cl, a suppressor and a brightener, when Creutz teaches similar copper electroplating baths (cols. 5-6, Examples).

Applicants state that these claims are also patentable because even if the modification were made, the combination of references does not disclose or suggest the express requirement to increase the overall chloride content and the overall sulfur content of the copper deposit. In particular, neither Barstad et al. nor Creutz et al. discuss problems related to creep deformation or the advantages which could be gained from purposefully introducing chloride impurity in the copper deposit. It is not surprising that Creutz et al., directed to plating through holes in PCB substrates, do not discuss the problem because creep deformation is not a serious problem in copper in through holes in PCB substrates.

In response, the reason or motivation to modify the reference may often suggest

what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by the Applicants. *In re Linter* 458 F.2d 1013, 173 USPQ 560 (CCPA 1972); *In re Dillon* 919 F.2d 688, 16 USPQ2d 1897 (Fed. Cir. 1990), *cert. denied*, 500 US 904 (1991); and MPEP § 2144.

Applicants state that Barstad et al. are silent, or even in some respects teach away from including a component in their copper electroplating bath which purposefully introduces impurities in the copper deposit where they express a preference for plating copper which has an absence of "...voids, inclusions, and seams)..."

In response, Creutz teaches an electroplating bath composition that is physically the same as the electroplating bath composition recited in the claims 1 and 17. If the composition is physically the same, it must have the same properties (MPEP § 2112.01(II)).

Applicants state that while it may be tempting to conclude that the proposed combination of Creutz et al. and Barstad et al. would have inherently increased the chloride and sulfur content of the deposit, this cannot fairly be maintained in view of the disparate nature of the respective teachings as to how the particular reaction product is used. In particular, Creutz et al. added the reaction product in a quantity of just 0.5 mg/L (Example II, col. 6, line 12). Examples III and IV used only 1 and 0.4 ppm of the reaction

product. There is no indication this would increase the chloride and sulfur content of the deposit as required by claim 1.

In response, claims 1 and 17, lines 8-9 of each claim, recite "an effective amount of a defect reducing agent". This amount is arbitrary so as long as it (a) reduces a rate of recrystallization and grain growth in the copper deposit, and/or (b) increases a chloride content and a sulfur content of the copper deposit. The (a) reduction and/or (b) increase is arbitrary so as long as it happens to some degree. There is no evidence that electroplating with the electroplating baths disclosed by Creutz would not have done this to some degree.

Applicants state that in the present situation there is no technical basis to make this conclusion in view of the lack of any statement by Creutz et al. that they increased chloride content and in view of the low quantities in which the reaction product was added.

In response, there is no requirement that the effect be expressly articulated in one or more of the references. References are evaluated by what they collectively suggest to one versed in the art, rather than by their specific disclosures. *In re Simon* 174 USPQ 114 (CCPA 1972); *In re Richman* 165 USPQ 509, 514 (CCPA 1970).

Claims 1 and 17, lines 8-9 of each claim, recite "an effective amount of a defect reducing agent". This amount is arbitrary so as long as it (a) reduces a rate of recrystallization and grain growth in the copper deposit, and/or (b) increases a chloride

content and a sulfur content of the copper deposit. The (a) reduction and/or (b) increase is arbitrary so as long as it happens to some degree. There is no evidence that electroplating with the electroplating bath disclosed by Creutz would not have done this to some degree.

Creutz teaches an electroplating bath composition that is physically the same as the electroplating bath composition recited in the claims 1 and 17. If the composition is physically the same, it must have the same properties (MPEP § 2112.01(II)).

II. Claims **17 and 72-73** have been rejected under 35 U.S.C. 103(a) as being unpatentable over **Creutz, deceased et al.** (US Patent No. 4,110,176) in combination with **Barstad et al.** (US Patent No. 6,444,110 B2).

The rejection of claims 17 and 72-73 under 35 U.S.C. 103(a) as being unpatentable over Creutz, deceased et al. in combination with Barstad et al. is as applied in the Office Action dated June 16, 2006 and incorporated herein. The rejection has been maintained for the reasons as discussed above.

Applicants' remarks have been fully considered but they are not deemed to be persuasive.

Response to Amendment

Claim Rejections - 35 USC § 103

Claim **74** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Creutz,**

deceased et al. (US Patent No. 4,110,176) in combination with **Barstad et al.** (US Patent No. 6,444,110 B2) as applied to claims 1-7 and 65-71 above, and further in view of **Pedersen et al.** (US Patent No. 6,673,216 B2).

Creutz and Barstad are as applied above and incorporated herein.

The method of Creutz and Barstad differs from the instant invention because they do not disclose wherein the semiconductor integrated circuit device substrate is a silicon wafer, as recited in claim 74.

Barstad teaches semiconductor integrated circuits (col. 3, lines 55-56).

Like Barstad, Pedersen teaches electrochemical processing a microelectronic workpiece. Pedersen teaches that semiconductor integrated circuits and other microelectronic devices typically include a substrate or workpiece, such as a silicon wafer, and one or more metal layers disposed on the workpiece (col. 1, lines 25-28).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the semiconductor integrated circuit device substrate described by Barstad with wherein the semiconductor integrated circuit device substrate is a silicon wafer because semiconductor integrated circuits and other microelectronic devices typically include a substrate or workpiece, such as a silicon wafer, and one or more metal layers disposed on the workpiece as taught by Pedersen (col. 1, lines 25-28).

Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

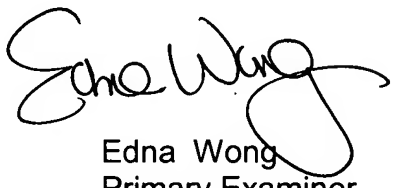
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edna Wong whose telephone number is (571) 272-1349. The examiner can normally be reached on Mon-Fri 7:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Edna Wong
Primary Examiner
Art Unit 1753

EW
February 4, 2007